The LTC®2756 is an 18-bit multiplying serial-input, current-output digital-to-analog converter. LTC2756A provides full 18-bit performance—INL and DNL of ±1 LSB maximum—over temperature without any adjustments. 18-bit monotonicity is guaranteed in all performance grades. This SoftSpan™ DAC operates from a single 3V to 5V supply and offers six output ranges (up to ±10V) that can be programmed through the 3-wire SPI serial interface or pin-strapped for operation in a single range.

Any on-chip register (including DAC output-range settings) can be read for verification in just one instruction cycle; and if you change register content, the altered register will be automatically read back during the next instruction cycle.

Voltage-controlled offset and gain adjustments are also provided; and the power-on reset circuit and CLR pin both reset the DAC output to 0V regardless of output range.

**APPLICATIONS**

- Instrumentation
- Medical Devices
- Automatic Test Equipment
- Process Control and Industrial Automation
**LTC2756**

**ABSOlute MAXIMUM RATINGS**

(Notes 1, 2)

<table>
<thead>
<tr>
<th>Description</th>
<th>Maximum Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{OUT1}, I_{OUT2}$ to GND</td>
<td>$\pm 0.3V$</td>
</tr>
<tr>
<td>$R_{IN}, R_{COM}, REF, R_{FB}, R_{OFS}, V_{OSADJ}$ to GND</td>
<td>$\pm 18V$</td>
</tr>
<tr>
<td>$V_{DD}$ to GND</td>
<td>$–0.3V$ to $7V$</td>
</tr>
<tr>
<td>Digital Inputs to GND</td>
<td>$–0.3V$ to $7V$</td>
</tr>
<tr>
<td>Digital Outputs to GND</td>
<td>$–0.3V$ to $V_{DD}$ $+0.3V$ (Max $7V$)</td>
</tr>
</tbody>
</table>

**Operating Temperature Range**

- LTC2756C: $0°C$ to $70°C$
- LTC2756I: $–40°C$ to $85°C$

**Maximum Junction Temperature**

- $150°C$

**Storage Temperature Range**

- $–65°C$ to $150°C$

**Lead Temperature (Soldering, 10 sec)**

- $300°C$

**ORDER INFORMATION**

http://www.linear.com/product/LTC2756#orderinfo

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC2756BCG#PBF</td>
<td>LTC2756BCG#TRPBF</td>
<td>LTC2756G</td>
<td>28-Lead Plastic SSOP</td>
<td>$0°C$ to $70°C$</td>
</tr>
<tr>
<td>LTC2756BIG#PBF</td>
<td>LTC2756BIG#TRPBF</td>
<td>LTC2756G</td>
<td>28-Lead Plastic SSOP</td>
<td>$–40°C$ to $85°C$</td>
</tr>
<tr>
<td>LTC2756ACG#PBF</td>
<td>LTC2756ACG#TRPBF</td>
<td>LTC2756G</td>
<td>28-Lead Plastic SSOP</td>
<td>$0°C$ to $70°C$</td>
</tr>
<tr>
<td>LTC2756AIG#PBF</td>
<td>LTC2756AIG#TRPBF</td>
<td>LTC2756G</td>
<td>28-Lead Plastic SSOP</td>
<td>$–40°C$ to $85°C$</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.
**ELECTRICAL CHARACTERISTICS**  
$V_{DD} = 5V, V(R_{IN}) = 5V$ unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC2756</th>
<th>LTC2756A</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>Static Performance</td>
<td>Resolution</td>
<td>●</td>
<td>18</td>
<td>18</td>
<td>Bits</td>
</tr>
<tr>
<td></td>
<td>Monotonicity</td>
<td>●</td>
<td>18</td>
<td>18</td>
<td>Bits</td>
</tr>
<tr>
<td></td>
<td>DNL</td>
<td>●</td>
<td>±1</td>
<td>±0.25</td>
<td>±1</td>
</tr>
<tr>
<td></td>
<td>INL</td>
<td>●</td>
<td>±2</td>
<td>±0.5</td>
<td>±1</td>
</tr>
<tr>
<td></td>
<td>GE</td>
<td>Gain Error</td>
<td>●</td>
<td>±40</td>
<td>±5</td>
</tr>
<tr>
<td></td>
<td>Gain Error Temperature Coefficient</td>
<td>ΔGain/ΔTemp</td>
<td>●</td>
<td>±0.25</td>
<td>±0.25</td>
</tr>
<tr>
<td></td>
<td>BZE</td>
<td>Bipolar Zero Error</td>
<td>●</td>
<td>±24</td>
<td>±25</td>
</tr>
<tr>
<td></td>
<td>Bipolar Zero Temperature Coefficient</td>
<td>●</td>
<td>±0.15</td>
<td>±0.15</td>
<td>ppm/°C</td>
</tr>
<tr>
<td></td>
<td>Unipolar Zero-Scale Error</td>
<td>Unipolar Ranges (Note 3)</td>
<td>●</td>
<td>±0.03</td>
<td>±3.2</td>
</tr>
<tr>
<td></td>
<td>PSR</td>
<td>Power Supply Rejection</td>
<td>$V_{DD} = 5V, ±10%$</td>
<td>●</td>
<td>±1.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3V, ±10%$</td>
<td>●</td>
<td>±4</td>
<td>±0.2</td>
</tr>
<tr>
<td></td>
<td>$I_{LKG}$</td>
<td>$I_{OUT1}$ Leakage Current</td>
<td>$T_A = 25°C$</td>
<td>●</td>
<td>±0.05</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>●</td>
<td>±5</td>
<td>±5</td>
</tr>
</tbody>
</table>

$V_{DD} = 5V, V(R_{IN}) = 5V$ unless otherwise specified. The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Analog Pins</td>
<td>Reference Inverting Resistors</td>
<td>(Note 4)</td>
<td>●</td>
<td>16</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>$R_{REF}$</td>
<td>DAC Input Resistance</td>
<td>(Notes 5, 6)</td>
<td>●</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>$R_{FB}$</td>
<td>Feedback Resistors</td>
<td>(Note 6)</td>
<td>●</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>$R_{OFS}$</td>
<td>Bipolar Offset Resistors</td>
<td>(Note 6)</td>
<td>●</td>
<td>16</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>$R_{VOSADJ}$</td>
<td>Offset Adjust Resistors</td>
<td></td>
<td></td>
<td>1024</td>
<td>1280</td>
</tr>
<tr>
<td></td>
<td>$R_{GEADJ}$</td>
<td>Gain Adjust Resistors</td>
<td>(Note 6)</td>
<td>●</td>
<td>2048</td>
<td>2560</td>
</tr>
<tr>
<td></td>
<td>$C_{OUT1}$</td>
<td>Output Capacitance</td>
<td>Full-Scale</td>
<td></td>
<td>90</td>
<td>40</td>
</tr>
</tbody>
</table>

### Dynamic Performance

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Output Settling Time</td>
<td>Span Code = 0000, 10V Step, To ±0.0004% FS (Note 7)</td>
<td></td>
<td>2.1</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>Glitch Impulse</td>
<td>$V_{DD} = 5V$ (Note 8)</td>
<td></td>
<td>2</td>
<td></td>
<td>nV•s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3V$ (Note 8)</td>
<td></td>
<td>0.4</td>
<td></td>
<td>nV•s</td>
</tr>
<tr>
<td></td>
<td>Digital-to-Analog Glitch Impulse</td>
<td>$V_{DD} = 5V$ (Note 9)</td>
<td></td>
<td>2.6</td>
<td></td>
<td>nV•s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3V$ (Note 9)</td>
<td></td>
<td>0.6</td>
<td></td>
<td>nV•s</td>
</tr>
<tr>
<td></td>
<td>Reference Multiplying BW</td>
<td>0V to 5V Range, Code = Full Scale, −3dB Bandwidth</td>
<td></td>
<td>1</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>Multiplying Feedthrough Error</td>
<td>0V to 5V Range, $V_{REF} = ±10V, 10kHz$ Sine Wave</td>
<td></td>
<td>0.4</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>THD</td>
<td>Total Harmonic Distortion (Note 10) Multiplying</td>
<td></td>
<td>–108</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>Output Noise Voltage Density</td>
<td>(Note 11) at $I_{OUT1}$</td>
<td></td>
<td>13</td>
<td></td>
<td>nV/√Hz</td>
</tr>
</tbody>
</table>
# LTC2756

## Electrical Characteristics

V<sub>DD</sub> = 5V, V(R<sub>IN</sub>) = 5V unless otherwise specified. The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T<sub>A</sub> = 25°C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Supply Voltage</td>
<td></td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Supply Current, V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Digital Inputs = 0V or V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>0.5</td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Digital Input Low Voltage</td>
<td>4.5V &lt; V&lt;sub&gt;DD&lt;/sub&gt; ≤ 5.5V</td>
<td>0.8</td>
<td>0.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7V ≤ V&lt;sub&gt;DD&lt;/sub&gt; ≤ 4.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>Digital Input High Voltage</td>
<td>3.3V ≤ V&lt;sub&gt;DD&lt;/sub&gt; ≤ 5.5V</td>
<td>2.4</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7V ≤ V&lt;sub&gt;DD&lt;/sub&gt; &lt; 3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hysteresis Voltage</td>
<td></td>
<td></td>
<td>0.1</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Digital Input Current</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = GND to V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>±1</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Digital Input Capacitance</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 0V (Note 12)</td>
<td>6</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = 200μA</td>
<td>2.7V ≤ V&lt;sub&gt;DD&lt;/sub&gt; ≤ 5.5V</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; – 0.4</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;DL&lt;/sub&gt;</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 200μA</td>
<td>2.7V ≤ V&lt;sub&gt;DD&lt;/sub&gt; ≤ 5.5V</td>
<td></td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

## Timing Characteristics

The • denotes specifications that apply over the full operating temperature range, otherwise specifications are at T<sub>A</sub> = 25°C.

### V<sub>DD</sub> = 4.5V to 5.5V

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;1&lt;/sub&gt;</td>
<td>SDI Valid to SCK Set-Up</td>
<td></td>
<td>7</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;2&lt;/sub&gt;</td>
<td>SDI Valid to SCK Hold</td>
<td></td>
<td>7</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;3&lt;/sub&gt;</td>
<td>SCK High Time</td>
<td></td>
<td>11</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;4&lt;/sub&gt;</td>
<td>SCK Low Time</td>
<td></td>
<td>11</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;5&lt;/sub&gt;</td>
<td>CS/LD Pulse Width</td>
<td></td>
<td>9</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;6&lt;/sub&gt;</td>
<td>LSB SCK High to CS/LD High</td>
<td></td>
<td>4</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;7&lt;/sub&gt;</td>
<td>CS/LD Low to SCK Positive Edge</td>
<td></td>
<td>4</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;8&lt;/sub&gt;</td>
<td>CS/LD High to SCK Positive Edge</td>
<td></td>
<td>4</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;9&lt;/sub&gt;</td>
<td>SRO Propagation Delay</td>
<td>C&lt;sub&gt;LOAD&lt;/sub&gt; = 10pF</td>
<td>18</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;10&lt;/sub&gt;</td>
<td>CLR Pulse Width Low</td>
<td></td>
<td>36</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;11&lt;/sub&gt;</td>
<td>LDAC Pulse Width Low</td>
<td></td>
<td>15</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;12&lt;/sub&gt;</td>
<td>CLR Low to RFLAG Low</td>
<td>C&lt;sub&gt;LOAD&lt;/sub&gt; = 10pF (Note 12)</td>
<td>50</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;13&lt;/sub&gt;</td>
<td>CS/LD High to RFLAG High</td>
<td>C&lt;sub&gt;LOAD&lt;/sub&gt; = 10pF (Note 12)</td>
<td>40</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>40</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
</tbody>
</table>

### V<sub>DD</sub> = 2.7V to 3.3V

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;1&lt;/sub&gt;</td>
<td>SDI Valid to SCK Set-Up</td>
<td></td>
<td>9</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;2&lt;/sub&gt;</td>
<td>SDI Valid to SCK Hold</td>
<td></td>
<td>9</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;3&lt;/sub&gt;</td>
<td>SCK High Time</td>
<td></td>
<td>15</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;4&lt;/sub&gt;</td>
<td>SCK Low Time</td>
<td></td>
<td>15</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;5&lt;/sub&gt;</td>
<td>CS/LD Pulse Width</td>
<td></td>
<td>12</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;6&lt;/sub&gt;</td>
<td>LSB SCK High to CS/LD High</td>
<td></td>
<td>5</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
**TIMING CHARACTERISTICS**  

The • denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_7$</td>
<td>CS/LD Low to SCK Positive Edge</td>
<td>•</td>
<td>5</td>
<td>5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_8$</td>
<td>CS/LD High to SCK Positive Edge</td>
<td>•</td>
<td>5</td>
<td>5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_9$</td>
<td>SRO Propagation Delay</td>
<td>$C_{LOAD} = 10pF$</td>
<td>•</td>
<td>26</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{10}$</td>
<td>CLR Pulse Width Low</td>
<td>•</td>
<td>60</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{11}$</td>
<td>LDAÇ Pulse Width Low</td>
<td>•</td>
<td>20</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{12}$</td>
<td>CLR Low to RFLAG Low</td>
<td>$C_{LOAD} = 10pF$ (Note 12)</td>
<td>•</td>
<td>70</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{13}$</td>
<td>CS/LD High to RFLAG high</td>
<td>$C_{LOAD} = 10pF$ (Note 12)</td>
<td>•</td>
<td>60</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SCK Frequency</td>
<td>50% Duty Cycle (Note 13)</td>
<td>•</td>
<td>25</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 3:** Calculation from feedback resistance and $I_{OUT1}$ leakage current specifications; not production tested. In most applications, unipolar zero-scale error is dominated by contributions from the output amplifier.

**Note 4:** Input resistors measured from $R_{IN}$ to $R_{COM}$; feedback resistors measured from $R_{COM}$ to $REF$.

**Note 5:** DAC input resistance is independent of code.

**Note 6:** Parallel combination of the resistances from the specified pin to $I_{OUT1}$ and from the specified pin to $I_{OUT2}$.

**Note 7:** Using LT1468 with $C_{FEEDBACK} = 27pF$. A ±0.0004% settling time of 1.8µs can be achieved by optimizing the time constant on an individual basis. See Application Note 120, 1ppm Settling Time Measurement for a Monolithic 18-Bit DAC.

**Note 8:** Measured at the major carry transition, 0V to 5V range. Output amplifier: LT1468; $C_{FB} = 50pF$.

**Note 9:** Full-scale transition; $REF = 0V$.

**Note 10:** $REF = 6V_{RMS}$ at 1kHz. 0V to 5V range. DAC code = FS. Output amplifier = LT1468.

**Note 11:** Calculation from $V_n = \sqrt{4kTRB}$, where $k = 1.38E-23 J/°K$ (Boltzmann constant), $R = \text{resistance (Ω)}$, $T = \text{temperature (°K)}$, and $B = \text{bandwidth (Hz)}$. 0V to 5V Range; zero-, mid-, or full-scale.

**Note 12:** Guaranteed by design; not production tested.

**Note 13:** When using SRO, maximum SCK frequency $f_{MAX}$ is limited by SRO propagation delay $t_9$ as follows:

$$f_{MAX} = \left( \frac{1}{2(t_9 + t_S)} \right)$$

where $t_S$ is the setup time of the receiving device.

For more information visit www.linear.com/LTC2756
TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 5V, V(RIN) = 5V, TA = 25°C, unless otherwise noted.
TYPICAL PERFORMANCE CHARACTERISTICS

\( V_{DD} = 5V, V(R_{IN}) = 5V, T_A = 25^\circ C, \) unless otherwise noted.

**INL vs V\(_{DD}\)**

- +INL
- -INL

\( V_{DD} (V) \)

\[ \begin{array}{c|ccccccc}
2.5 & 3 & 3.5 & 4 & 4.5 & 5 & 5.5 \\
\hline
0.5 & 0.4 & 0.3 & 0.2 & 0.1 & 0.0 & -0.1 \\
\end{array} \]

**DNL vs V\(_{DD}\)**

- +DNL
- -DNL

\( V_{DD} (V) \)

\[ \begin{array}{c|ccccccc}
2.5 & 3 & 3.5 & 4 & 4.5 & 5 & 5.5 \\
\hline
0.5 & 0.4 & 0.3 & 0.2 & 0.1 & 0.0 & -0.1 \\
\end{array} \]

**Supply Current vs Logic Input Voltage**

- CLR, LDAC, SDI, SCK, CS/LD TIED TOGETHER

\( V_{DD} = 5V \)

\( V_{DD} = 3V \)

\[ \begin{array}{c|ccccccc}
0 & 1 & 2 & 3 & 4 & 5 \\
\hline
0.5 & 1 & 2 & 3 & 4 & 5 \\
\end{array} \]

**Logic Threshold vs Supply Voltage**

- RISING
- FALLING

\( V_{DD} (V) \)

\[ \begin{array}{c|ccccccc}
2.5 & 3 & 3.5 & 4 & 4.5 & 5 & 5.5 \\
\hline
1.5 & 2 & 2.5 & 3 & 3.5 & 4 & 4.5 \\
\end{array} \]

**Supply Current vs Update Frequency**

\( V_{DD} = 5V \)

\( V_{DD} = 3V \)

\[ \begin{array}{c|ccccccc}
1 & 10 & 100 & 1k & 10k & 100k & 1M \\
\hline
0.0001 & 0.001 & 0.01 & 0.1 & 1 & 10 & 100 \\
\end{array} \]

**Mid-Scale Glitch (V\(_{DD}\) = 3V)**

- LT1468 AMP; C\(_{FEEDBACK}\) = 20pF
- 0V TO 10V STEP
- \( V_{REF} = -10V \); SPAN CODE = 0000
- \( t_{SETTLE} = 1.8\mu s \) to 0.0004\% (18 BITS)

**Mid-Scale Glitch (V\(_{DD}\) = 5V)**

- LT1468 OUTPUT AMPLIFIER
- \( C_{FEEDBACK} = 50pF \)
- RISING MAJOR CARRY TRANSITION.
- FALLING TRANSITION IS SIMILAR OR BETTER.
PIN FUNCTIONS

$R_{OFF}$ (Pin 1): Bipolar Offset Resistor. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at $R_{IN}$ (Pin 5).

REF (Pin 2): DAC Reference Input, and Feedback Resistor for the Reference Inverting Amplifier. The external reference inverting amplifier sees as its load the 10k DAC reference input resistance in parallel with the 20k feedback resistor. For normal operation tie this pin to the output of the reference inverting amplifier (see the Typical Applications section). Typically 5V; accepts up to ±15V.

$R_{COM}$ (Pin 3): Virtual Ground Point for the On-Chip Reference Inverting Resistors. These precision-matched 20k resistors are included on the chip to facilitate generation of the negative reference voltage needed to produce a positive output polarity. They are connected internally from $R_{IN}$ to $R_{COM}$ and from $R_{COM}$ to REF (see Block Diagram). For normal operation tie $R_{COM}$ to the negative input of the external reference inverting amplifier (see the Typical Applications section).

$GEA_{DJ}$ (Pin 4): Gain Adjust Pin. This control pin can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±2048 LSB for a voltage input range of ±$V_{IN}$ (i.e., ±5V for a 5V reference input). Tie to ground if not used.

$R_{IN}$ (Pin 5): Input Resistor for Reference Inverting Amplifier. The 20k input resistor is connected internally from $R_{IN}$ to $R_{COM}$. For normal operation tie $R_{IN}$ to the external reference voltage (see the Typical Applications section). Typically 5V; accepts up to ±15V.

GND (Pins 6, 8, 13, 15, 16, 24): Ground; tie to ground.

$I_{OUT2}$ (Pin 7): Current Output Complement. Tie to ground via a clean, low-impedance path.

CS/LD (Pin 9): Synchronous Chip Select and Load Input Pin. A logic low on this pin enables SDI, SCK and SRO (Pins 10, 11 and 12) for input and output of serial data.

SDI (Pin 10): Serial Data Input. Data is clocked in on the rising edge of the serial clock (SCK, Pin 11) when $CS/LD$ (Pin 9) is low.

SCK (Pin 11): Serial Clock.

SRO (Pin 12): Serial Readback Output. Data is clocked out on the falling edge of SCK. Readback data begins clocking out after the first byte is clocked in. SRO is an active output only when the chip is selected (i.e., when $CS/LD$ is low). Otherwise SRO presents a high-impedance output in order to allow other parts to control the bus.

$V_{DD}$ (Pin 14): Positive Supply Input; 2.7V ≤ $V_{DD}$ ≤ 5.5V. Bypass with a 0.1μF low-ESR capacitor to ground.

CLR (Pin 17): Asynchronous Clear Input. When this pin is low, all DAC registers (both code and span) are cleared to zero. The DAC output is cleared to zero volts.

$R_{FLAG}$ (Pin 18): Reset Flag Output. An active low output is asserted when there is a power-on reset or a clear event. Returns high when an Update command is executed.

M-SPAN (Pin 19): Manual Span Control Pin. M-SPAN is used in conjunction with pins S0, S1 and S2 (Pins 20, 21 and 22) to configure the DAC for operation in a single, fixed output range.

To configure the part for manual-span use, tie M-SPAN directly to $V_{DD}$. The active output range is then set via hardware pin strapping of pins S2, S1 and S0 (rather than through the SPI port); and Write and Update commands have no effect on the active output span.

To configure the part for SoftSpan use, tie M-SPAN directly to GND. The output ranges are then individually controllable through the SPI port; and pins S2, S1 and S0 have no effect.

See Manual Span Configuration in the Operation section. M-SPAN must be connected either directly to GND (SoftSpan configuration) or to $V_{DD}$ (manual-span configuration).
**PIN FUNCTIONS**

**S0 (Pin 20):** Span Bit 0 Input. In Manual Span mode (M-SPAN tied to VDD), pins S0, S1 and S2 are pin-strapped to select a single fixed output range. These pins must be tied to either GND or VDD even if they are unused.

**S1 (Pin 21):** Span Bit 1 Input. In Manual Span mode (M-SPAN tied to VDD), pins S0, S1 and S2 are pin-strapped to select a single fixed output range. These pins must be tied to either GND or VDD even if they are unused.

**S2 (Pin 22):** Span Bit 2 Input. In Manual Span mode (M-SPAN tied to VDD), pins S0, S1 and S2 are pin-strapped to select a single fixed output range. These pins must be tied to either GND or VDD even if they are unused.

**LDAC (Pin 23):** Asynchronous DAC Load Input. When LDAC is logic low, the DAC is updated (CS/LD must be high).

**VOSADJ (Pin 25):** Offset Adjust Pin. This control pin can be used to null unipolar offset or bipolar zero error. The offset-voltage delta is inverted and attenuated such that a 5V control voltage applied to VOSADJ produces ΔVOS = –2048 LSB in any output range (assumes a 5V reference voltage at RIN). See *System Offset and Gain Adjustments* in the Operation section. Tie to ground if not used.

**IOUT1 (Pin 26):** Current Output Pin. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier (see the Typical Applications section).

**RFB (Pins 27, 28):** Feedback Resistor. For normal operation tie both pins to the output of the I/V converter amplifier (see the Typical Applications section). The DAC output current from IOUT1 flows through the feedback resistor to the RFB pins.
LTC2756

BLOCK DIAGRAM

For more information www.linear.com/LTC2756
### OPERATION

#### Output Ranges

The LTC2756 is a current-output, serial-input precision multiplying DAC with selectable output ranges. Ranges can either be programmed in software for maximum flexibility—the DAC can be programmed to any one of six output ranges—or hardwired through pin-strapping. Two unipolar ranges are available (0V to 5V and 0V to 10V), and four bipolar ranges (±2.5V, ±5V, ±10V and −2.5V to 7.5V). These ranges are obtained when an external precision 5V reference is used. The output ranges for other reference voltages are easy to calculate by observing that each range is a multiple of the external reference voltage. The ranges can then be expressed: 0 to 1×, 0 to 2×, ±0.5×, ±1×, ±2×, and −0.5× to 1.5×.

#### Manual Span Configuration

Multiple output ranges are not needed in some applications. To configure the LTC2756 to operate in a single span without additional operational overhead, tie the M-SPAN pin directly to VDD. The active output range is then set via hardware pin strapping of pins S2, S1 and S0 (rather than through the SPI port); and Write and Update commands have no effect on the active output span. See Figure 1 and Table 2.

Tie the M-SPAN pin to ground for normal SoftSpan operation.

---

#### Input and DAC Registers

The LTC2756 has two sets of double-buffered registers—one set for the code data, and one for the output range of the DAC—plus one readback register, for a total of five registers. Double buffering provides the capability to simultaneously update the span (output range) and code, which allows smooth voltage transitions when changing output ranges.

Each set of double-buffered registers comprises an Input register and a DAC register.

Input register: The Write operation shifts data from the SDI pin into a chosen Input register. The Input registers are holding buffers; Write operations do not affect the DAC outputs.

DAC register: The Update operation copies the contents of an Input register to its associated DAC register. The contents of a DAC register directly updates the associated DAC output voltage or output range.

Note that updates always include both Code and Span register sets; but the values held in the DAC registers will only change if the associated Input register values have previously been altered via a Write operation.

---

**Figure 1. Using M-SPAN to Configure the LTC2756 for Single-Span Operation (±10V Range Shown)**
### Serial Interface
When the CS/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (SCK pin). The loading sequence required for the LTC2756 is one byte consisting of a 4-bit command word (C3 C2 C1 C0) and four zeros, then three bytes (24 bits) of data.

When writing a code, the code data is left (MSB) justified; so that the 24-bit data field consists of 18 code bits followed by 6 don’t-care bits.

When writing an output range, the span data should occupy the last 4 bits of the second data byte, ordered S3 through S0. Figure 2 shows the SDI input word syntax for writing.

When CS/LD is low, the SRO pin (Serial Readback Output) is an active output. The readback data begins after the first byte has been shifted in to SDI. SRO outputs a logic low from the falling edge of CS/LD until the Readback data begins.

When CS/LD is high, the SRO pin presents a high impedance (three-state) output.

LDAC is an asynchronous update pin. When LDAC is taken low, the DAC is updated with code and span data (data in the Input buffers is copied into the DAC buffers). CS/LD must be high during this operation; otherwise LDAC is locked out and will have no effect. The use of LDAC is functionally identical to the serial input command.

The codes for the command (C3-C0) are defined in Table 1.

### Readback
In addition to the Code and Span register sets, the LTC2756 has one Readback register. At the end of every instruction cycle, the contents of one of the on-chip registers is copied into the Readback register and serially shifted out through the SRO pin.

Readback data always appears in the 24-bit data field, starting on the falling SCK edge immediately after the first byte is shifted in on SDI. When reading a code, code data occupies the first 18 bits of the 24-bit field; and the span bits are the last four bits of the second data byte when checking the output range. In both cases, all other bits in the 24-bit data field are filled by zeros. Figure 2 shows the input and readback sequences.

The data outputted by SRO is always in the same position and sequence as the input data. Note, however, that this means that the SRO data shifts out one-half clock cycle earlier than the corresponding bit shifting in on SDI. For example, code bit D9, which is shifted in to SDI on the rising edge of SCK clock 17, is clocked out of SRO on the falling edge of clock 16. This allows D9 to be clocked to an external microprocessor on the rising edge of clock 17.

For Read commands, the requested data is shifted out of SRO in the 3-byte (24-bit) data field immediately after the command byte. There is no instruction-cycle latency for Read commands; the data shifts out in the same instruction cycle in which it was requested.

For non-read (i.e., Write and/or Update) commands, SRO automatically shifts out the contents of the buffer that was acted upon in the preceding command. This “rolling readback” default mode of operation can dramatically reduce the number of instruction cycles needed, since most commands can be verified during subsequent commands with no additional overhead. A conceptual flow diagram is shown in Figure 3. Table 1 shows, for each antecedent command, which register (‘readback pointer’) will be copied into the Readback register and outputted from SRO during the following instruction cycle.

### Span Readback in Manual Span Configuration
If the Span DAC register is chosen for readback, SRO responds by outputting the actual output span; this is true whether the LTC2756 is configured for SoftSpan (M-SPAN tied to GND) or manual span (M-SPAN tied to VDD).

In SoftSpan configuration, SRO outputs the span code from the Span DAC register (programmed through the SPI port). In manual span configuration, the active output range is controlled by pins S2, S1 and S0, so SRO outputs the logic values of these pins. The span code bits S2, S1 and S0 always appear in the same order and positions in the SRO output sequence; see Figure 2.
### Table 1. Command Codes

<table>
<thead>
<tr>
<th>CODE</th>
<th>COMMAND</th>
<th>READING BACK POINTER—CURRENT INPUT WORD W0</th>
<th>READING BACK POINTER—NEXT INPUT WORD W+1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 1 0</td>
<td>Write Span</td>
<td>Set by Previous Command</td>
<td>Input Span Register</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>Write Code</td>
<td>Set by Previous Command</td>
<td>Input Code Register</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>Update</td>
<td>Set by Previous Command</td>
<td>DAC Span Register</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>Write Span; Update</td>
<td>Set by Previous Command</td>
<td>DAC Span Register</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>Write Code; Update</td>
<td>Set by Previous Command</td>
<td>DAC Code Register</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>Read Input Span Register</td>
<td>Input Span Register</td>
<td>Input Span Register</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>Read Input Code Register</td>
<td>Input Code Register</td>
<td>Input Code Register</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>Read DAC Span Register</td>
<td>DAC Span Register</td>
<td>DAC Span Register</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>Read DAC Code Register</td>
<td>DAC Code Register</td>
<td>DAC Code Register</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>No Operation</td>
<td>Set by Previous Command</td>
<td>DAC Code Register</td>
</tr>
</tbody>
</table>

Codes not shown are reserved—do not use.

### Table 2. Span Codes

<table>
<thead>
<tr>
<th>SPAN</th>
<th>CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>Unipolar 0V to 5V</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>Unipolar 0V to 10V</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>Bipolar –5V to 5V</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>Bipolar –10V to 10V</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>Bipolar –2.5V to 2.5V</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>Bipolar –2.5V to 7.5V</td>
</tr>
</tbody>
</table>

Codes not shown are reserved—do not use.
Figure 2. Serial Input and Output Sequences
Figure 3. Rolling Readback Example
Examples

1. Load ±5V range with the output at 0V. Note that since span and code are updated together, the output stays at 0V throughout the example.

   a) \( \overline{CS}/LD \downarrow \). Clock SDI:
      
      \[
      00100000 \text{XXXXXXX XXXX0010 XXXXXXXX}
      \]

   b) \( \overline{CS}/LD \uparrow \). Span Input register – range set to bipolar ±5V.

   c) \( \overline{CS}/LD \downarrow \). Clock SDI:
      
      \[
      00110000 10000000 00000000 00XXXXXX
      \]

   d) \( \overline{CS}/LD \uparrow \). Code Input register – code set to mid-scale.

   e) \( \overline{CS}/LD \downarrow \). Clock SDI:
      
      \[
      01000000 \text{XXXXXXX XXXXXX XXXXXXXX}
      \]

   f) \( \overline{CS}/LD \uparrow \). Update code and range. Alternatively steps e and f could be replaced with LDAC "L".

2. Load ±10V range with the output at 5V, changing to –5V.

   a) \( \overline{CS}/LD \downarrow \). Clock SDI:
      
      \[
      00110000 11000000 00000000 00XXXXXX
      \]

   b) \( \overline{CS}/LD \uparrow \). Code Input register set to ¾-scale code.

   c) \( \overline{CS}/LD \downarrow \). Clock SDI:
      
      \[
      01100000 \text{XXXXXXX XXXX0011 XXXXXXXX}
      \]

   d) \( \overline{CS}/LD \uparrow \). Span Input register set to ±10V range. Update code and range. Output goes to 5V.

   g) \( \overline{CS}/LD \downarrow \). Clock SDI:
      
      \[
      01100000 01000000 00000000 00XXXXXX
      \]

   h) \( \overline{CS}/LD \uparrow \). Code Input register set to ¼-scale code. Update code and range (note update does not change range, since no new range has been written). Output goes to –5V.

3. Write and update mid-scale code in 0V to 10V range \((V_{OUT} = 5V)\) using readback to check the contents of the Input registers before updating.

   a) \( \overline{CS}/LD \downarrow \). Clock SDI:
      
      \[
      00110000 10000000 00000000 00XXXXXX
      \]

   b) \( \overline{CS}/LD \uparrow \). Code Input register set to mid-scale.

   c) \( \overline{CS}/LD \downarrow \). Clock SDI:
      
      \[
      00100000 \text{XXXXXXX XXXX0001 XXXXXXXX}
      \]

   d) \( \overline{CS}/LD \uparrow \). Span Input register set to 0V to 10V range.

   e) \( \overline{CS}/LD \downarrow \). Clock SDI:
      
      \[
      10100000 \text{XXXXXXX XXXXXX XXXXXXXX}
      \]

   f) \( \overline{CS}/LD \uparrow \). Span Input register set to 0V to 10V range.

   g) \( \overline{CS}/LD \downarrow \). Clock SDI:
      
      \[
      01000000 \text{XXXXXXX XXXXXX XXXXXXXX}
      \]

   h) \( \overline{CS}/LD \uparrow \). Update code and range. Output goes to 5V.
OPERATION

System Offset and Reference Adjustments

Many systems require compensation for overall system offset. This may be an order of magnitude or more greater than the offset of the LTC2756, which is so low as to be dominated by external output amplifier errors even when using the most precise op amps.

The offset adjust pin \( V_{OSADJ} \) can be used to null unipolar offset or bipolar zero error. The offset change expressed in LSB is the same for any output range:

\[
\Delta V_{OS}[\text{LSB}] = -\frac{V(V_{OSADJ})}{V(R_{IN})} \cdot 2048
\]

A 5V control voltage applied to \( V_{OSADJ} \) produces \( \Delta V_{OS} = -2048 \) LSB in any output range, assuming a 5V reference voltage at \( R_{IN} \).

In voltage terms, the offset delta is attenuated by a factor of 32, 64 or 128, depending on the output range. (These functions hold regardless of reference voltage.)

- \( \Delta V_{OS} = -\left(\frac{1}{128}\right)V_{OSADJ} \)  
  [0V to 5V, ±2.5V spans]
- \( \Delta V_{OS} = -\left(\frac{1}{64}\right)V_{OSADJ} \)  
  [0V to 10V, ±5V, −2.5V to 7.5V spans]
- \( \Delta V_{OS} = -\left(\frac{1}{32}\right)V_{OSADJ} \)  
  [±10V span]

The gain error adjust pins \( GE_{ADJ} \) can be used to null gain error or to compensate for reference errors. The gain error change expressed in LSB is the same for any output range:

\[
\Delta GE = \frac{V(GE_{ADJ})}{V(R_{IN})} \cdot 2048
\]

The gain-error delta is non-inverting for positive reference voltages.

Note that this pin compensates the gain by altering the inverted reference voltage \( V(\text{REF}) \). In voltage terms, the \( V(\text{REF}) \) delta is inverted and attenuated by a factor of 128.

\( \Delta V(\text{REF}) = -(\frac{1}{128})GE_{ADJ} \)

The nominal input range of these pins is ±5V; other voltages of up to ±15V may be used if needed. However, do not use voltages divided down from power supplies; reference-quality, low-noise inputs are required to maintain the best DAC performance.

The \( V_{OSADJ} \) pin has an input impedance of 1.28MΩ. It should be driven with a Thevenin-equivalent impedance of 10k or less to preserve the settling performance of the LTC2756. The \( V_{OSADJ} \) pin should be shorted to GND if not used.

The \( GE_{ADJ} \) pin has an input impedance of 2.56MΩ, and is intended for use with fixed reference voltages only. It should be shorted to GND if not used.

Power-On Reset and Clear

When power is first applied to the LTC2756, the DAC powers up in unipolar 5V mode (S3 S2 S1 S0 = 0000). All internal DAC registers are reset to 0 and the DAC output initializes to zero volts.

If the part is configured for manual span operation, the DAC will be set into the pin-strapped range at the first Update command. This allows the user to simultaneously update span and code for a smooth voltage transition into the chosen output range.

When the \( CLR \) pin is taken low, a system clear results. The DAC buffers are reset to 0 and the DAC output is reset to zero volts. The Input buffers are left intact, so that any subsequent Update command (including the use of LDAC) restores the DAC to its previous state.

If \( CLR \) is asserted during an instruction, i.e., when CS/LD is low, the instruction is aborted. Integrity of the relevant Input buffers is not guaranteed under these conditions, therefore the contents should be checked using readback or replaced.

The \( RFLAG \) pin is used as a flag to notify the system of a loss of data integrity. The \( RFLAG \) output is asserted low at power-up, system clear, or if the supply \( V_{DD} \) dips below approximately 2V; and stays asserted until any valid Update command is executed.
Op Amp Selection

Because of the extremely high accuracy of the 18-bit LTC2756, careful thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Tables 3 and 4 contain equations for evaluating the effects of op amp parameters on the LTC2756’s accuracy when programmed in a unipolar or bipolar output range. These are the changes the op amp can cause to the INL, DNL, unipolar offset, unipolar gain error, bipolar zero and bipolar gain error.

Table 5 contains a partial list of LTC precision op amps recommended for use with the LTC2756. The easy-to-use design equations simplify the selection of op amps to meet the system’s specified error budget. Select the amplifier from Table 5 and insert the specified op amp parameters in Table 4. Add up all the errors for each category to determine the effect the op amp has on the accuracy of the part. Arithmetic summation gives an (unlikely) worst-case effect. A root-sum-square (RMS) summation produces a more realistic estimate.
Op amp offset contributes mostly to DAC output offset and gain error, and has minimal effect on INL and DNL. For example, consider the LTC2756 in unipolar 5V output range. (Note that for this example, the LSB size is 19µV.) An op amp offset of 35µV will cause 1.8LSB of output offset, and 1.8LSB of gain error; but 0.4LSB of INL, and just 0.1LSB of DNL.

While not directly addressed by the simple equations in Tables 3 and 4, temperature effects can be handled just as easily for unipolar and bipolar applications. First, consult an op amp’s data sheet to find the worst-case $V_{OS}$ and $I_B$ over temperature. Then, plug these numbers in the $V_{OS}$ and $I_B$ equations from Table 4 and calculate the temperature-induced effects.

For applications where fast settling time is important, Application Note 120, 1ppm Settling Time Measurement for a Monolithic 18-Bit DAC, offers a thorough discussion of 18-bit DAC settling time and op amp selection.

**Recommendations**

For DC or low-frequency applications, the LTC1150 is the simplest 18-bit accurate output amplifier. An auto-zero amp, its exceptionally low offset (10µV max) and offset drift (0.01µV/°C) make nulling unnecessary. For swings above 8V, add an LT®1010 buffer to boost the load current capability. The settling of auto-zero amps is a special case; see Application Note 120, 1ppm Settling Time Measurement for a Monolithic 18-Bit DAC, Appendix E, for details.

The LT1012 and LT1001 are good intermediate output-amp solutions that achieve moderate speed and good accuracy. They are also excellent choices for the reference inverting amplifier in fixed-reference applications.

For high speed applications, the LT1468 settles in 2.1µs. Note that the 75µV max offset will degrade the INL at the DAC output by up to 0.9LSB. For high-speed applications demanding higher precision, the amplifier offset can be nulled with a digital potentiometer.

Figure 5 shows a composite output amplifier that achieves fast settling (8µs) and very low offset (3µV max) without offset nulling. This circuit offers high open-loop gain (1000V/mV min), low input bias current (0.15nA max), fast slew rate (25V/µs min), and a high gain-bandwidth product (30MHz typ). The high speed path consists of an LTC6240HV, which is an 18MHz ultralow bias current amplifier, followed by an LT1360, a 50MHz fast-slew amplifier which provides additional gain and the ability to swing to ±10V at the output. Compensation is taken from the output of the LTC6240HV, allowing the use of a much larger compensation capacitor than if taken after the gain-of-five stage. An LTC2054HV auto-zero amplifier senses the voltage at $I_{OUT1}$ and drives the non-inverting input of the LTC6240HV to eliminate the offset of the high speed path. The 100:1 attenuator and input filter reduce the low frequency noise in this stage while maintaining low DC offset.

**Precision Voltage Reference Considerations**

Much in the same way selecting an operational amplifier for use with the LTC2756 is critical to the performance of the system, selecting a precision voltage reference also requires due diligence. The output voltage of the LTC2756 is directly affected by the voltage reference; thus, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 18-bit applications: output voltage initial tolerance, output voltage temperature coefficient and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with low output voltage initial tolerance, like the LTC6655 (±0.025%), minimizes the gain error caused by the reference; however, a calibration sequence that corrects for system zero- and full-scale error is always recommended. A reference’s output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit’s INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.
Table 6. Partial List of LTC Precision References Recommended for Use with the LTC2756 with Relevant Specifications

<table>
<thead>
<tr>
<th>REFERENCE</th>
<th>INITIAL TOLERANCE</th>
<th>TEMPERATURE DRIFT</th>
<th>0.1Hz to 10Hz NOISE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT1019A-5, -10</td>
<td>±0.05% max</td>
<td>5ppm/°C max</td>
<td>12µV p-p</td>
</tr>
<tr>
<td>LT1236A-5, -10</td>
<td>±0.05% max</td>
<td>5ppm/°C max</td>
<td>3µV p-p</td>
</tr>
<tr>
<td>LT1460A-5, -10</td>
<td>±0.075% max</td>
<td>10ppm/°C max</td>
<td>20µV p-p</td>
</tr>
<tr>
<td>LT1790A-2.5</td>
<td>±0.05% max</td>
<td>10ppm/°C max</td>
<td>12µV p-p</td>
</tr>
<tr>
<td>LTC6652A-5</td>
<td>±0.05% max</td>
<td>5ppm/°C max</td>
<td>2.8ppm p-p</td>
</tr>
<tr>
<td>LTC6655A-2.5, -5</td>
<td>±0.025% max</td>
<td>2ppm/°C max</td>
<td>0.25ppm p-p</td>
</tr>
</tbody>
</table>

As precision DAC applications move to 18-bit performance, reference output voltage noise may contribute a dominant share of the system’s noise floor. This in turn can degrade system dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references like the LT1236 or LTC6655 produce low output noise in the 0.1Hz to 10Hz region, well below the 18-bit LSB level in 5V or 10V full-scale systems. However, as the circuit bandwidths increase, filtering the output of the reference may be required to minimize output noise.

**Grounding**

As with any high-resolution converter, clean grounding is important. A low-impedance analog ground plane is necessary, as are star grounding techniques. Keep the board layer used for star ground continuous to minimize ground resistances; that is, use the star-ground concept without using separate star traces. The IOUT2 pin is of particular importance; INL will be degraded by the code-dependent currents carried by IOUT2 if voltage drops to ground are allowed to develop. The best strategy here is to tie the pins to the star ground plane by multiple vias located directly underneath the part. Alternatively, the pin may be routed to the star ground point if necessary; route a trace of no more than 30 squares of 1oz copper.

In the rare case in which neither of these alternatives is practicable, a force/sense amplifier should be used as a ground buffer (see Figure 4). Note, however, that the voltage offset of the ground buffer amp directly contributes to the effects on accuracy specified in Table 4 under ‘VOS1’. The combined effects of the offsets can be calculated by substituting the total offset from IOUT1 to IOUT2 for VOS1 in the equations.
Figure 4. If a Low-Impedance GND Plane Is Unavailable, Drive IOUT2 with a Force/Sense Amplifier As Shown. Use Circuit A to Minimize Impact on Settling Time, or Circuit B for Lower Power Consumption and Better Accuracy.
PACKAGE DESCRIPTION
Please refer to http://www.linear.com/product/LTC2756#packaging for the most recent package drawings.

G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING NOT TO SCALE
4. DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
5. **DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

Recommended Solder Pad Layout

For more information www.linear.com/LTC2756
## REVISION HISTORY

<table>
<thead>
<tr>
<th>REV</th>
<th>DATE</th>
<th>DESCRIPTION</th>
<th>PAGE NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>12/16</td>
<td>Updated amplifier part numbers.</td>
<td>19, 24</td>
</tr>
</tbody>
</table>
**TYPICAL APPLICATION**

![Circuit Diagram](image)

**Figure 5. Composite Amplifier Provides Both 18-Bit Precision and Fast Settling**

**RELATED PARTS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC2757</td>
<td>Single Parallel 18-Bit IOUT SoftSpan DAC</td>
<td>±1LSB INL/DNL, Software-Selectable Ranges, 7mm × 7mm LQFP-48 Package</td>
</tr>
<tr>
<td>LTC1592</td>
<td>Single Serial 16-/14-/12-Bit IOUT SoftSpan DACs</td>
<td>±1LSB INL/DNL, Software-Selectable Ranges, 16-Lead SSOP Package</td>
</tr>
<tr>
<td>LTC2751</td>
<td>Single Parallel 16-/14-/12-Bit IOUT SoftSpan DACs</td>
<td>±1LSB INL/DNL, Software-Selectable Ranges, 5mm × 7mm QFN-38 Package</td>
</tr>
<tr>
<td>LTC1597/LTC1591</td>
<td>Single Parallel 16-/14-Bit IOUT DACs</td>
<td>±1LSB INL/DNL, Integrated 4-Quadrant Resistors, 28-Lead SSOP Package</td>
</tr>
<tr>
<td>LTC2758</td>
<td>Dual Serial 18-Bit IOUT SoftSpan DAC</td>
<td>±1LSB INL/DNL, Software-Selectable Ranges, 7mm × 7mm LQFP-48 Package</td>
</tr>
<tr>
<td>LTC2754</td>
<td>Quad Serial 16-/12-Bit IOUT SoftSpan DACs</td>
<td>±1LSB INL/DNL, Software-Selectable Ranges, 7mm × 8mm QFN-52 Package</td>
</tr>
<tr>
<td>LTC2704</td>
<td>Quad Serial 16-/14-/12-Bit VOUT SoftSpan DACs</td>
<td>±1LSB INL/DNL, Software-Selectable Ranges, Integrated Amplifiers</td>
</tr>
<tr>
<td>LTC2641/LTC2642</td>
<td>16-/14-/12-Bit VOUT DACs</td>
<td>±1LSB INL/DNL, 0.5nV•s Glitch, 1µs Settling, 3mm × 3mm DFN</td>
</tr>
</tbody>
</table>

**References**

- LTC6655A-2.5/LTC6655A-5: Low Drift Precision Buffered Reference
  - 0.025% Max Tolerance, 2ppm/°C Max, 0.25ppm/°C Max, 0.1Hz to 10Hz Noise

- LT1236A-5/LT1236A-10: Precision Reference
  - 0.05% Max Tolerance, 5ppm/°C Max, 3µVp-p, 0.1Hz to 10Hz Noise

- LT1460A-5/LT1460A-10: Micropower Precision Series Reference
  - 0.075% Max Tolerance, 10ppm/°C Max, 20µVp-p, 0.1Hz to 10Hz Noise

- LT1790A-2.5: Micropower Low Dropout Reference
  - 0.05% Max Tolerance, 10ppm/°C Max, 12µVp-p, 0.1Hz to 10Hz Noise

- LTC6652A-5: Precision Low Drift Low Noise Buffered Reference
  - 0.05% Max Tolerance, 5ppm/°C Max, 2.8ppm/°C Max, 0.1Hz to 10Hz Noise

**Amplifiers**

- LTC1150: Zero-Drift Op Amp with Internal Capacitors
  - 10µV Max Offset, ±16V High Voltage Operation, 1.8µVp-p Noise

- LT1012: Precision Op Amp
  - 25µV Max Offset, 100µA Max Input Current, 0.5µVp-p Noise, 380µA Supply Current

- LT1001: Precision Op Amp
  - 25µV Max Offset, 0.3µVp-p Noise, High Output Drive

- LT1468: Single 16-Bit Accurate Op Amp
  - 900ns Settling, 90MHz GBW, 22V/µs Slew Rate, 75µV Max Offset