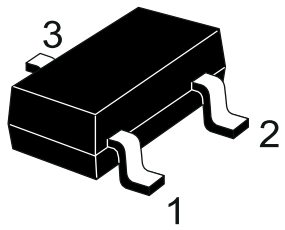
STR2P3LLH6

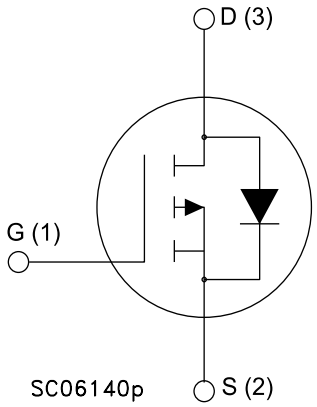
P-channel 30 V, 0.048 Ω typ., 2 A STripFET™ H6 Power MOSFET in a SOT-23 package

Datasheet - production data



SOT-23

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STR2P3LLH6	30 V	0.056 Ω @ 10 V	2 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order codes	Marking	Package	Packaging
STR2P3LLH6	2K3L	SOT-23	Tape and reel

For the P-channel MOSFET the actual polarity of the voltages and the current must be reversed.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_{pcb} = 25 °C	2	A
I_D	Drain current (continuous) at T_{pcb} = 100 °C	1.2	A
I_{DM} (1)	Drain current (pulsed)	8	A
P_{TOT}	Total dissipation at T_{pcb} = 25 °C	0.35	W
T_J	Operating junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

Notes:

(1)Pulse width limited by safe operating area

Table 3: Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb, single operation	357	°C/W

Notes:

(1)When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

For the P-channel MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 250 µA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 30 V, T_J = 125 °C			1	µA
I_{GSS}	Gate body leakage current	V_{GS} = 0, V_{GS} = ±20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1 A V_{GS} = 4.5 V, I_D = 1 A		0.048 0.075	0.056 0.09	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f=1 MHz V_{GS} = 0	-	639	-	pF
C_{oss}	Output capacitance		-	79	-	
C_{rss}	Reverse transfer capacitance		-	52	-	
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 2 A V_{GS} = 4.5 V	-	6	-	nC
Q_{gs}	Gate-source charge		-	1.9	-	
Q_{gd}	Gate-drain charge		-	2.1	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 2 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	5.4	-	ns
t_r	Rise time		-	5	-	
$t_{d\ (off)}$	Turn-off delay time		-	19.2	-	
t_f	Fall time		-	3.4	-	

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 2 A, V_{GS} = 0	-	-	1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 2 A, di/dt = 100 A/µs, V_{DD}= 24 V, T_J = 150 °C	-	-	11.2	ns
Q_{rr}	Reverse recovery charge		-	-	3.5	nC
I_{RRM}	Reverse recovery current		-	-	0.6	A

Notes:

(1)Pulsed: pulse duration=300µs, duty cycle 1.5%

For the P-channel MOSFET the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

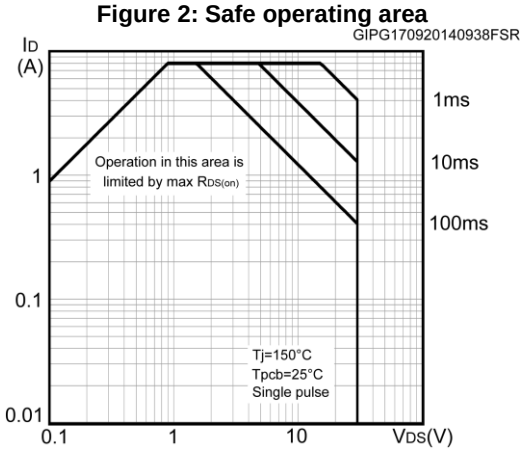


Figure 3: Thermal impedance

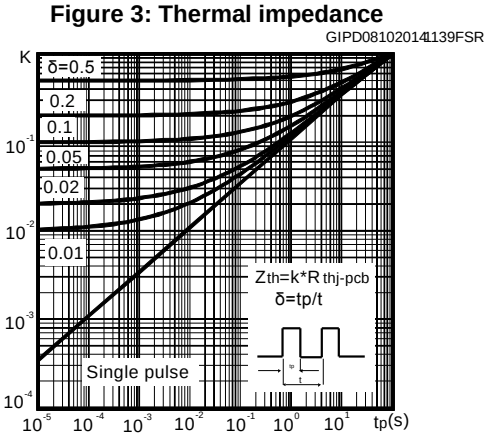


Figure 4: Output characteristics

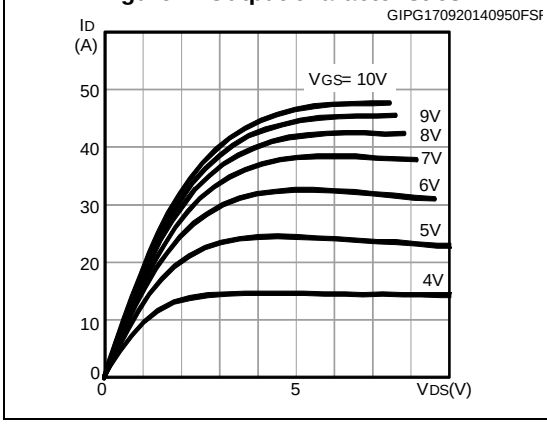


Figure 5: Transfer characteristics

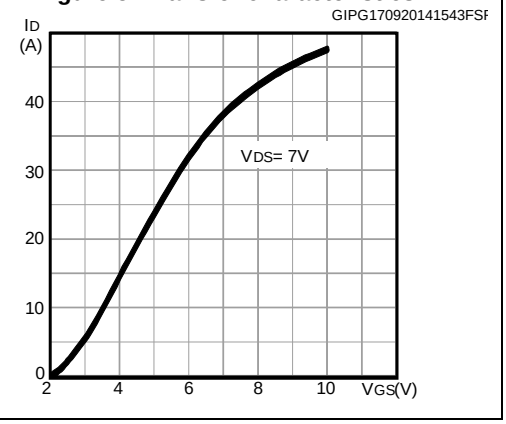


Figure 6: Gate charge vs gate-source voltage

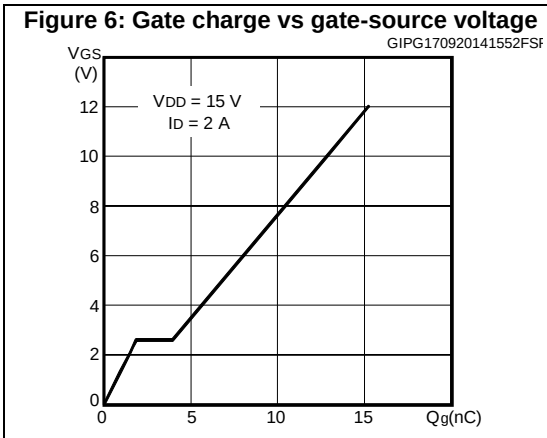


Figure 7: Static drain-source on-resistance

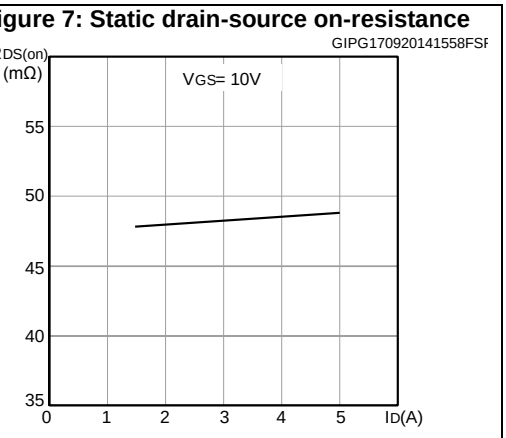


Figure 8: Normalized V(BR)DSS vs temperature

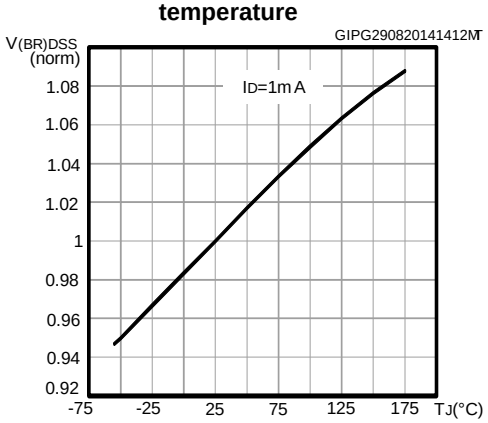


Figure 9: Capacitance variations

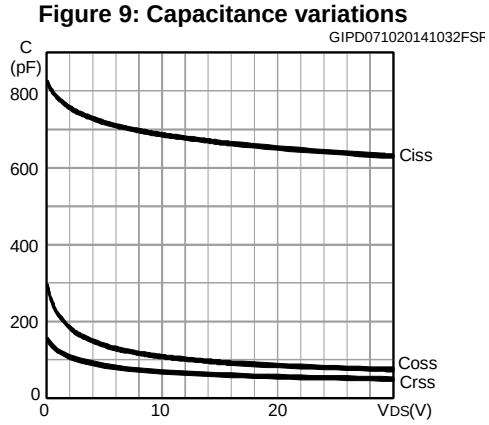


Figure 10: Normalized gate threshold voltage vs. temperature

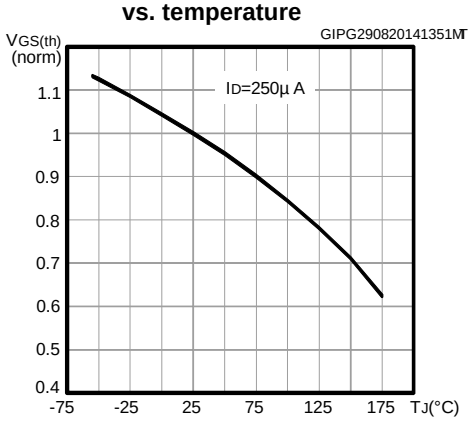


Figure 11: Normalized on-resistance vs. temperature

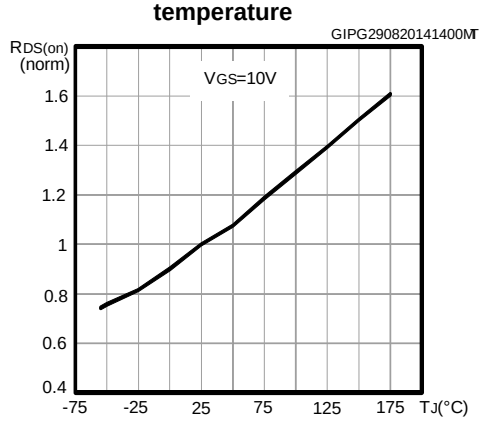
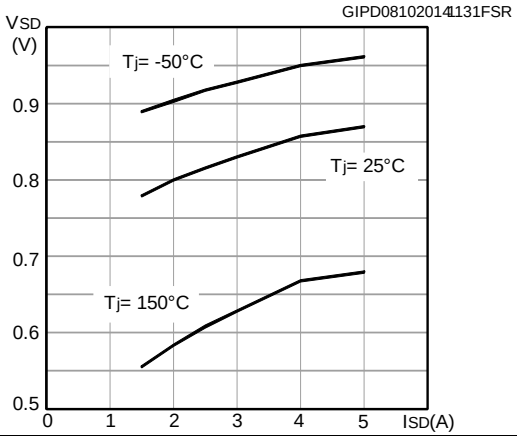


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

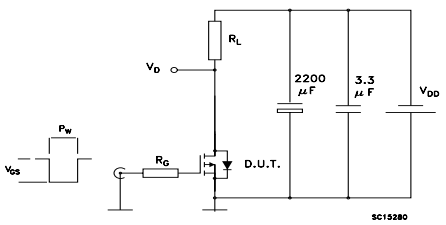


Figure 14: Gate charge test circuit

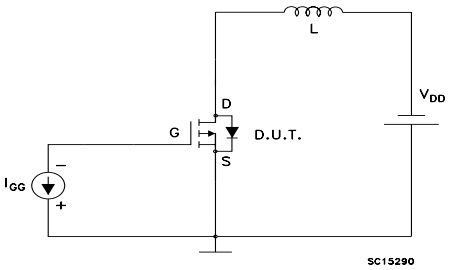
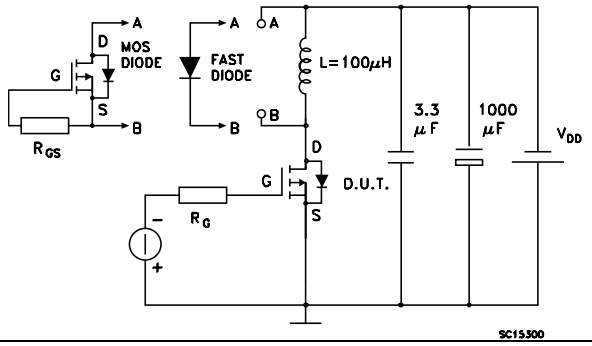


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 SOT-23

Figure 16: SOT-23 mechanical drawing

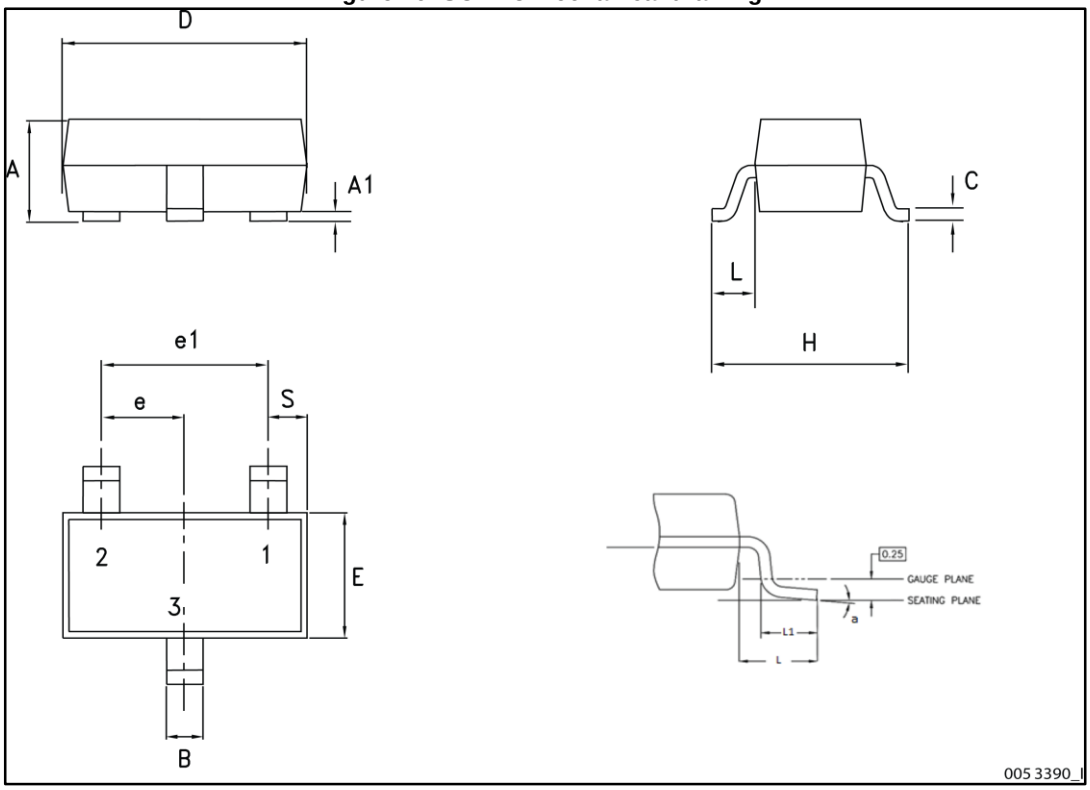
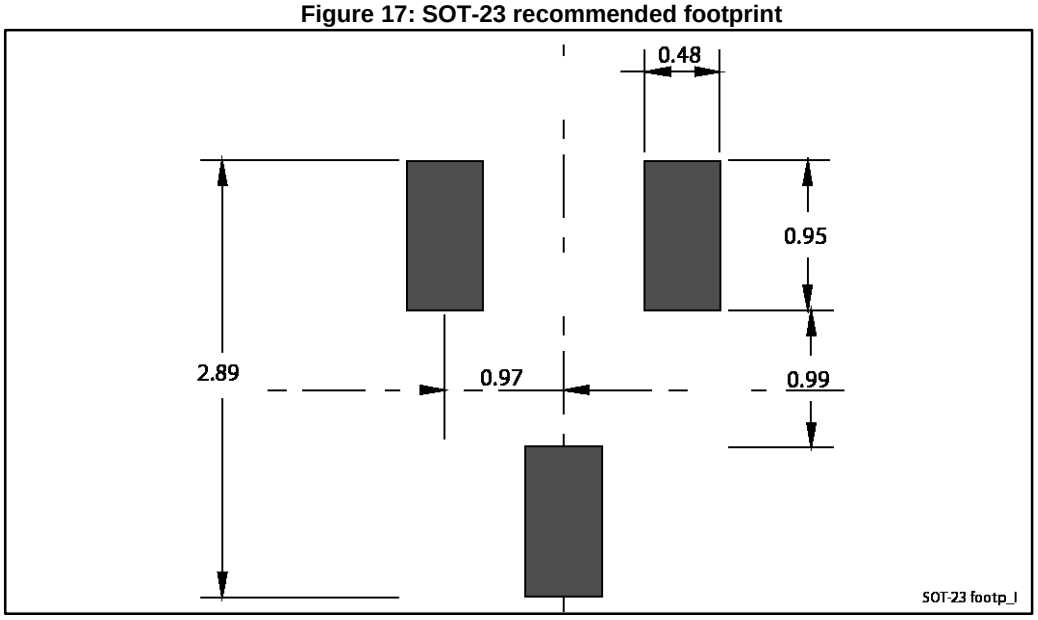


Table 8: SOT-23 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.89		1.40
A1	0		0.10
B	0.30		0.51
C	0.085		0.18
D	2.75		3.04
e	0.85		1.05
e1	1.70		2.10
E	1.20		1.75
H	2.10		3.00
L		0.60	
S	0.35		0.65
L1	0.25		0.55
a	0°		8°

Figure 17: SOT-23 recommended footprint



Dimensions are in mm.

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
09-May-2013	1	Initial release.
03-Nov-2014	2	Document status promoted from preliminary to production data. Added *Section 2.1: "Electrical characteristics (curves)"*. Minor text changes.

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